A1 Cancel

transistors and conductive types different from each other, said switch circuit being capable of cut off said logic circuit from a power supply line by simultaneously turning off said second and third transistors.

A2 NOT narrowing

Subject

3. (Amended) A logic operation circuit comprising:

a gate circuit which is connected between a virtual voltage line and a first reference voltage line and constituted by a plurality of first transistors; and

a second transistor which is connected between a second reference voltage line and said virtual voltage line and constituted by a transistor having a threshold voltage higher than that of each of said first transistors,

a source/drain terminal of each of said first transistors in said gate circuit being connected to either a source/drain terminal of another first transistor in said gate circuit or an output terminal of said gate circuit.

A3

5. (Amended) A logic operation circuit comprising:

a gate circuit which is connected between a first reference voltage line and a virtual voltage line and constituted by a plurality of first transistors;

Subject

a second transistor which is connected between said virtual voltage line and a second reference voltage line and has a threshold voltage higher than that of each of said first transistors; and

a third transistor which is connected between said first reference voltage line and an output terminal of said gate circuit and has a threshold voltage higher than that of each of said first transistors,

said second and third transistors being on/off-controlled in such a manner that one of them is turned on while the other is turned off and vice versa.

A4

8. (Amended) A logic operation circuit comprising:

a gate circuit which is constituted by a plurality of first transistors and connected to first and second virtual voltage lines;

a second transistor which is connected between a first reference voltage line and said first virtual voltage line and has a threshold voltage higher than each of said first transistors;

a third transistor which is connected between a second reference voltage line and said second virtual voltage line and has a threshold voltage higher than that of each of said first transistors; and

a storage circuit capable of holding output logic of said gate circuit, said storage circuit being composed of transistors having threshold voltages higher than that of each of said first transistors,

said second and third transistors being controlled to be OFF when said storage circuit holds said output logic of said gate circuit, and said second and third transistors being controlled to be ON when said storage circuit does not hold said output logic of said gate circuit.

9. (Amended) The logic operation circuit according to claim 8, wherein a source/drain terminal of said first transistor in said gate circuit is connected to a source/drain terminal of another first transistor in said gate, to said second reference voltage line circuit or an output terminal of said gate circuit.

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11. (Amended) A logic operation circuit comprising:

a gate circuit which is constituted by a plurality of first transistors and connected to first and second virtual voltage lines;

A5 Cont'd

a second transistor which is connected between a first reference voltage line and said first virtual voltage line and has a threshold voltage higher than that of each of said first transistors;

a third transistor which is connected between a second reference voltage line and said second virtual voltage line and has a threshold voltage higher than that of each of said first transistors; and

a bypass circuit which is connected to said gate circuit in parallel and constituted by a circuit substantially equal to said gate circuit by using a plurality of fourth transistors having a threshold voltage higher than that of each of said first transistors,

said bypass circuit being connected between said first and second reference voltage lines.

A6

14. (Amended) A flip flop comprising:

a first conduction interception circuit capable of switching conduction or shutoff between an input terminal and an output terminal;

a first storage circuit capable of holding output logic of said first conduction interception circuit;

a second conduction interception circuit which is capable of switching conduction or shutoff between an input terminal and an output terminal, and has said input terminal being connected to an output terminal of said first storage circuit; and

a second storage circuit capable of holding output logic of said second conduction interception circuit,

said first and second conduction interception circuits includes:

a gate circuit which is connected between a virtual voltage line and a first reference voltage line and constituted by a plurality of first transistors; and

a second transistor which is connected between a second reference voltage line and said virtual voltage line and constituted by a transistor having a threshold voltage higher than that of each of said first transistors,

a source/drain terminal of each of said first transistors in said gate circuit being connected to either a source/drain terminal of another first transistor in said gate circuit or an output terminal of said gate circuit, and

said first and second storage circuits being constituted by transistors having a threshold voltage higher than those of said gate circuits in said first and second conduction interception circuits.

15. (Amended) A flip flop comprising:

a first conduction interception circuit capable of switching conduction or shutoff between an input terminal and an output terminal;

a first storage circuit capable of holding output logic of said first conduction interception circuit;

a second conduction interception circuit which is capable of switching conduction or shutoff between an input terminal and an output terminal and has said input terminal being connected to an output terminal of said first storage circuit; and

a second storage circuit capable of holding output logic of said second conduction interception circuit,

said first and second conduction interception circuits includes:

a gate circuit which is connected between a first reference voltage line and a virtual voltage line and constituted by a plurality of first transistors;

a second transistor which is connected between said virtual voltage line and a second reference voltage line and has a threshold voltage higher than that of each of said first transistors; and

a third transistor which is connected between said first reference voltage line and an output terminal of said gate circuit and has a threshold voltage higher than that of each of said first transistors,

said second and third transistors being on/off-controlled in such a manner that one of them is turned on while the other is turned off and vice versa, and

said first and second storage circuits being constituted by transistors having a threshold voltage higher than those of said gate circuits in said first and second conduction interception circuits.

16. (Amended) A flip flop comprising:

a first conduction interception circuit capable of switching conduction or interception between an input terminal and an output terminal;

a first storage circuit capable of holding output logic of said first conduction interception circuit;

a second conduction interception circuit which is capable of switching conduction or interception between an input terminal and an output terminal and has said input terminal being connected to an output terminal of said first storage circuit;

and a second storage circuit capable of holding output logic of said second conduction interception circuit,

said first and second conduction interception circuits includes:

a gate circuit which is constituted by a plurality of first transistors and connected to first and second virtual voltage lines;

a second transistor which is connected between a first reference voltage line and said first virtual voltage line and has a threshold voltage higher than each of said first transistors;

a third transistor which is connected between a second reference voltage line and said second virtual voltage line and has a threshold voltage higher than that of each of said first transistors; and

a storage circuit capable of holding output logic of said gate circuit, said storage circuit being composed of transistors having threshold voltage higher than that of said first transistor,

said second and third transistors being controlled to be OFF when said storage circuit holds said output logic of said gate circuit, and said second and third transistors being controlled to be ON when said storage circuit does not hold said output logic of said gate circuit, and

said first and second storage circuits being constituted by transistors having a threshold voltage higher than those of said gate circuits in said first and second conduction interception circuits.

REMARKS

Favorable reconsideration of this application as presently amended in light of the following discussion is respectfully requested.

Claims 1-17 are presently active in this case. Claims 1, 3, 5, 8, 9, 11, and 14-16 have been amended by way of the present amendment.

In the outstanding office action, Figures 2, 9, and 10 were objected to for not being identified as "prior art;" claims 3, 5, 8, and 11 were objected to for not providing an antecedent basis for the limitation "said first transistor;" claims 1 and 2 were rejected under